REMARKS

This paper adds new claims 23-36. Claims 23-36 are supported by, for example, Figs. 13a-13c, Fig. 15, and column 11, line 1 through column 12, line 15.

Claims 1, 3, 5, 9, 12-15, 19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art Figs. 1, 2, and 5 in view of Inoue et al., U.S. Patent 6,333,522 (hereinafter "Inoue"). Applicants respectfully traverse the rejection.

Claim 1 recites "a p- and an n-electrode . . . attached to a same side of the light emitting device; and a superstrate, having a refractive index greater than a refractive index of sapphire, attached to the heterostructure."

Among Inoue and Applicants' Figs. 1, 2, and 5, the only device that could possibly have a superstrate with "a refractive index greater than a refractive index of sapphire" is Applicants' Fig. 2, which shows a device with a SiC growth substrate (not a superstrate). The Examiner argues on page 4 of the office action that Applicants' Figs. 1 and 5 "teach a superstrate having a 1.84 refractive index and Inoue et al teach a sapphire substrate having a 1.77 refractive index . . . Therefore, Admitted Prior Art Figures 1-2 and 5 teach a superstrate, having a refractive index greater the a [sic] refractive index of sapphire." Though Inoue and Applicants' Figs. 1 and 5 may disagree on the numeric value of the refractive index of sapphire, the superstrates in Inoue's devices and in Applicants Figs. 1 and 5 are still sapphire. A sapphire superstrate cannot possibly have "a refractive index greater than a refractive index of sapphire" as recited in claim 1. Accordingly, only Applicants' Fig. 2 teaches a structure that may satisfy the refractive index requirement of claim 1.

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Applicants' Fig. 2 does not have "a p- and an n-electrode . . . attached to a same side of the light emitting device." Applicants respectfully submit that it is not obvious to modify the device of Applicants' Fig. 2 to place both electrodes on a same side of the device as shown in Inoue's devices and in Applicants Figs. 1 and 5.

First, placing both electrodes on the same side of the device requires etching away a portion of the active region to form a mesa, as shown in Fig. 1. Removing part of the active region is expected to result in less light generated by the active region and therefore less light emitted from the device.

In addition, placing both electrodes on a same side of the device significantly complicates the process of mounting the device of a mount. For example, the large, backside n-electrode shown in Fig. 2 may be easily mounted on Inoue's Si diode element 2 by a large solder layer that may be inexpensively screen printed. The location of the contacts on opposite sides of the device means that the device does not need to be precisely placed on the solder layer, since there is no danger of shorting the two electrodes. In addition, the large area of the solder may efficiently conduct heat away from the device. In contrast, a device with both electrodes on the same side of the device requires much smaller connectors, which must be carefully placed in order to avoid shorting the two electrodes. Inoue describes microbumps with "a maximum lateral dimension ranging from 5 to 300 μm, and a height ranging from 5 to 50 μm." See column 2, lines 46-50 of Inoue. A person of skill in the art would expect that the careful placement required for such small connectors would increase the cost of mounting the device, and decrease the yield of devices that are suitably mounted without shorting the electrodes. In addition, small connectors may not conduct heat away from the device as efficiently as large connectors, resulting in diminished device performance.

A person of skill in the art would expect that combining Applicants' Fig. 2 device with devices having both electrodes on the same side would result in a device that costs more to produce at lower yields, and performs worse. Thus, there is no motivation to make such a combination. The only motivation supplied by the Examiner is a statement that "Admitted Prior Art Figures 1-2 and 5 and Inoue et al. are both from the same field of endeavor." As such, "the purpose disclosed by Inoue et al. would have been recognized in the pertinent art of

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Admitted Prior Art Figures 1-2 and 5." Such a generic statement that the two devices are from the same endeavor does not provide a motivation to endure the disadvantages, described above, from making such a combination.

Since it would not be obvious to modify Applicants' Fig. 2 to create the device of claim 1, claim 1 is allowable over Applicants Figs. 1, 2, and 5 and Inoue. Claims 3, 5, 9, 12-15, 19 and 21-22 depend from claim 1 and are thus allowable for at least the same reason.

In addition, with respect to claim 9, claim 9 recites "a portion of the p-electrode interposes portions of the n-electrode." Applicants can find no such teaching in Inoue. The Examiner states "Inoue et al. (Figure 13) teach a portion of the p-electrode 5 interposing portions of the n-electrodes 6 and 8." Fig. 13 of Inoue shows no such thing. In Fig. 13, p-electrode 5 is adjacent to n-electrode 6. Structure 8 is the "n-side electrode 8 on the Si diode element" (see column 22, line 61) not an n-electrode attached to the n-layer on the device, and as such does not satisfy claim 9. Claim 9 is therefore allowable over the combination of Figs. 1, 2, and 5 and Inoue for this additional reason.

With respect to claims 14 and 15, claim 14 recites "a p-conductive interface disposed between the p-interconnect and the p-electrode; and an n-conductive interface disposed between the n-interconnect and the n-electrode." Layer 73 of Fig. 8B is cited by the Examiner as being claim 14's p-conductive interface. As Applicants noted in the previous office action response, Fig. 8B clearly shows that layer 73 is beneath p-electrode 5, NOT between the p-interconnect and the p-electrode as required in claim 14. In addition, the portions of Inoue cited by the Examiner do not teach an n-conductive interface at all. In response, the Examiner states in the Response to Arguments section "Admitted Prior Art Figure 2 teaches a conductive interface (buffer) disposed between an interconnect (pad) and an electrode." Applicants respectfully note that there is no structure between the electrode (labeled "SEMI-TRANSPARENT NiAu") and the p bond-pad. Claims 14 and 15 are

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therefore allowable over the combination of Figs. 1, 2, and 5 and Inoue for this additional reason.

Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1, 2, and 5 in view of Krames et al., U.S. Publication No. US 2001/0000410 A1. Claims 4, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1, 2, and 5 in view of Krames et al., U.S. Patent 5,779,924. Claim 6 is rejected rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1, 2, and 5 in view of Furukawa et al., U.S. Patent 5,124,779. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1, 2, and 5 in view of Inoue and Shigihara et al., U.S. Patent 5,247,203. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figs. 1, 2, and 5 in view of Iranmanesh, U.S. Patent 5,521,440. None of the references cited by the Examiner remedy the deficiencies of Figures 1, 2, and 5 and Inoue with respect to claim 1. The claims rejected above all depend from claim 1 and are therefore allowable for at least the same reasons as claim 1.

Applicants thank the Examiner for allowing claims 10 and 16.

In view of the above arguments, Applicants respectfully request allowance of claims 1-36. Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

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